

A Novel Design of a Multi-layer 2:4 Decoder using Quantum-Dot Cellular Automata

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Abstract: The quantum-dot cellular automata (QCA) is considered as an alternative to complementary metal oxide semiconductor (CMOS) technology based on physical phenomena like Coulomb interaction to overcome the physical limitations of this technology. The decoder is one of the important components in digital circuits, which can be used in more comprehensive circuits such as full adders and memories. This paper proposes the 2:4 decoder using multilayer QCA technology. The multilayer decoder provides requirements of high-density devices with good computing power. The proposed 2:4 active high decoder reduces the clock phases to three, making the circuit faster than previous ones. Moreover, the number of cells and occupied space are significantly reduced, thus reducing power consumption. Multi-layer architecture has more reliability than coplanar architecture and allows for the easy layout change. The structure was simulated using QCA Designer software, and the simplified expressions and standard functions have been presented. The simulation results can be useful for using them in logic circuits.

Keywords: Quantum-Dot Cellular Automata, Nano Electronics, Majority Voter Gate, Active High Decoder.

1. INTRODUCTION

The goal of this digital design is the realization of the compact CMOS logic circuit. Since CMOS technology has limitations like diminishing dimensions and high power consumption [1-5], QCA technology is considered an alternative to CMOS [6]. The dimensions of the QCA cell greatly influence the design of QCA circuits, so that the smaller cell causes smaller connections and increases the density of devices. The progress of researches on QCA features requires special design processes.

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Wire crossing in QCA technology is one of the remarkable achievements of this technology. The wire crossing in digital design is vulnerable due to the nature of the quantum-dot cell, causing unwanted crosstalk between the two wires [7]. In classical QCA, the wire crossing can take place through coplanar cross through the rotation of cells of a wire or using multilayer crossovers. The multilayer design approach is more susceptible to accidental side effects. The middle layer of the multilayer structure is used to prevent any possible interference [8].

Unlike the CMOS integrated circuit (IC) which contains only the main layer containing active elements, in a multi-layered QCA architecture, each layer can be used as an active part in which a new circuit can be designed independently [9]. Multilayer architecture can be extracted directly from the perspective plan in addition to reducing the overall surface of the circuit, and therefore less chip surface is used compared to the coplanar model [10].

More complexity results in the increase of power consumption and the possibility of losing the signal. In this article, we designed the circuit with simple gates which reduce complexity and make signals more stable as well as power consumption decrease.

In addition, the previous QCA decoders have been designed in the coplanar method. We designed a multi-layer 2:4 decoder using the multilayer QCA technique. This design satisfies constraints like layer spacing and radius of influence with improved specifications and excellent results.

The organization of this paper is as follows: Section 2 contains the principles of the QCA. The introduction of the decoder and its significance are described in Section 3. Section 4 presents the proposed multilayer QCA decoder, and Section 5 contains simulation results and decoder performance evaluation. The final section concludes the article.

2. QUANTUM DOT CELLULAR AUTOMATA

A. Principles of QCA

The QCA cell with four quantum dots is shown in figure 1a. The cell consists of four quantum dots in the four corners of the square, where two electrons are injected [6]. There can be only one electron in any quantum dot. Coulomb repulsion forces cause the electrons to occupy opposite corners, leading to cells with polarization $P=+1$ (logic 1) and $P=-1$ (logic 0), shown in figure (1b).

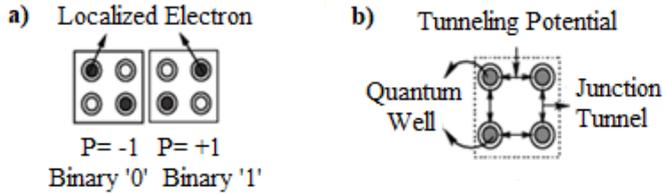


Fig. 1. a) QCA cell, b) QCA cell polarization [11].

Timing and synchronization in QCA are as shown in figure 2 using four distinct cascade clocks and periodic phases [12, 13].

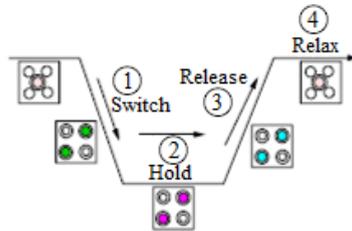


Fig. 2. QCA clocking [14].

One of the basic structures of QCA is the three input majority gate (MV₃) shown in figure 3, which is defined in accordance with equation (1):

$$Maj(a,b,c) = ab + bc + ac \tag{1}$$

The majority voter (MV₃) can also act as a two-input AND and OR gate, so that one of the inputs must be fixed to P = -1 and P = +1, respectively.

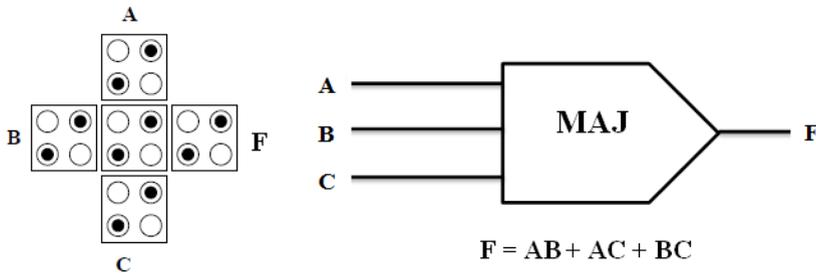


Fig. 3. Three input majority gate [15].

There is also a five-input majority voter [16] which is more complicated than the three-input one, which is difficult to implement in the circuit [17].

In QCA, there are two methods for the wire crossing, the coplanar method and the multilayer method [15]. The wire crossing in a coplanar method requires cells with two different directions of 45° and 90°. In a multilayer wire crossing

architecture, a cell can be placed on another cell, but in a different layer as in figure 4. In a multilayer architecture, different equations can be formed based on the location of the input and output of the majority voter [18, 19].

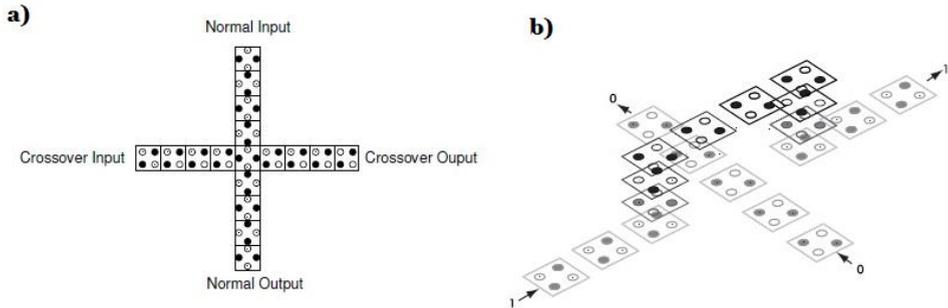


Fig. 4. Two crossover option in QCA. a) coplanar crossover, b) multilayer crossover [15].

Restrictions imposed due to the radius of the influence of a cell have been described in [16], where d is the distance that can affect a certain structure of QCA arrays.

Two layers of QCA are mutually interacting if $d = w + s$, where w is the cell width and s is the distance between two consecutive cells (figure 5).

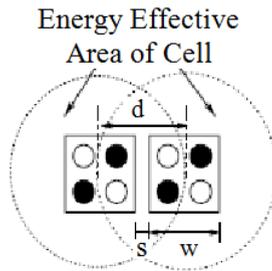


Fig. 5. Induced effect of cell [17].

B. QCA Designer

QCA Designer simulates the circuits based on QCA with layout tool rapidly and accurately. This software has been produced by the Walus Lab at the University of British Columbia [20]. The QCA Designer tool is able to design and simulation of QCA circuits by providing powerful CAD features available in more complex circuit design tools. QCA Designer inputs and outputs are the same input and outputs are used in equivalent logic circuits.

Input cells will have a polarization that is determined by the simulation engine. The input values will be set according to the Simulation Type. We can simulate all possible input combinations by choosing the exhaustive verification or select input vectors manually using a vector table. Output cells act just like

normal cells in that they are directly affected by their neighbors. The polarization of the output cells is recorded throughout the simulation and plotted in the graph dialog when the simulation is complete.

3. DECODER

Decoder plays an important role in computer architecture. They are used in various parts like random access memory (RAM) and look-up tables [21, 22]. In addition, all optical decoders can be used in optical logic circuits [23]. A decoder is a device which selects one of the output lines after activation. Most decoders have n inputs and 2^n outputs. The use of decoding in applications like multiplexing, 7-segment display, and memory address decoder is essential [24]. Table 1 shows the truth table of an active high 2:4 decoder.

TABLE I
TRUTH TABLE OF AN ACTIVE HIGH 2:4 DECODER

Input		Output			
A	B	F ₄	F ₃	F ₂	F ₁
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

4. PROPOSED MULTILAYER DECODER

In this design, four three-input majority voter gate has been used according to figure 6. One input of each majority voter gate has been fixed on logical 0 with a polarization $P = -1$, which results in the function of the majority gate as the AND gate.

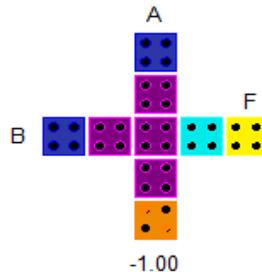


Fig. 6. AND Gate.

Decoder performance based on the majority voter gates for output production is as:

$$F_1 = MV_1(A, B, 0) \quad (2)$$

$$F_2 = MV_2(A', B, 0) \tag{3}$$

$$F_3 = MV_3(A, B', 0) \tag{4}$$

$$F_4 = MV_4(A, B, 0) \tag{5}$$

Different layers of the circuit are shown in figure7. The input data A and the data path A are applied to each of the MV_3 in the layer 1, in addition, the input data B is applied to the layer 3 and is transferred from the layer 3 to the prior to the majority voter device cell. The cells with constant inputs in each of the four majority voter gates are also placed in the layer1. Intermediate cells are placed in the layer 2. The top view of the circuit is depicted in figure 8. Input cells, fixed cells, and the data transmission path are placed in clock 0, the majority gate cells in clock 1 and the output cells are in clock 2, respectively.

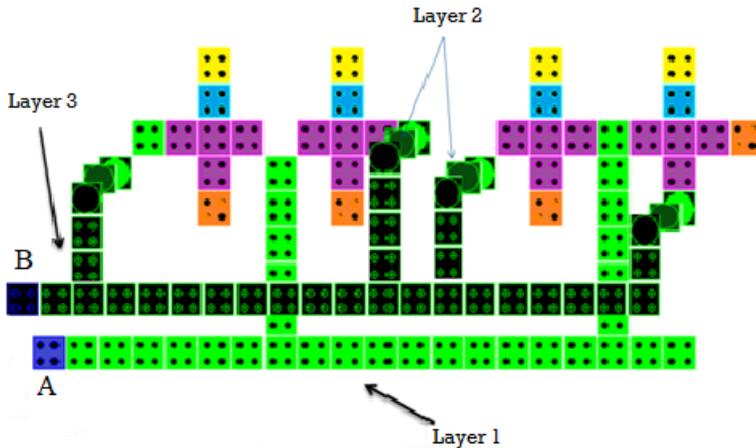


Fig. 7. Different layers of proposed 2:4 decoder.

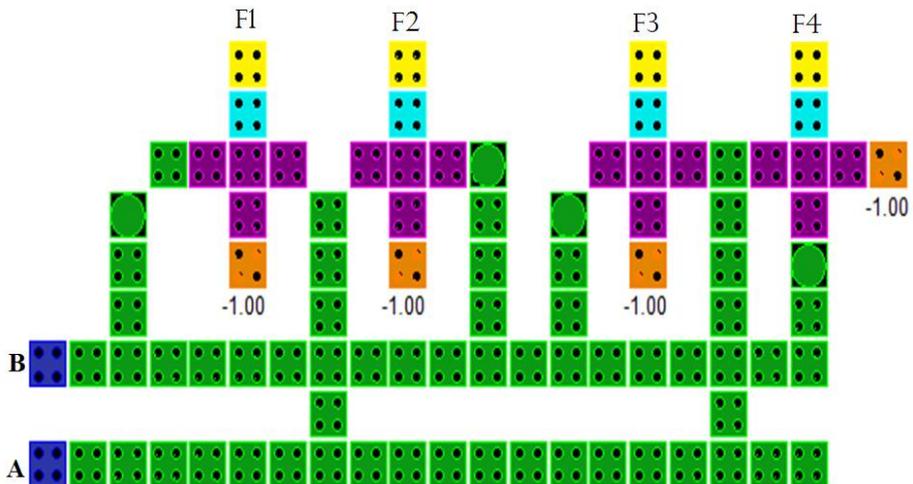


Fig. 8. Top view of proposed 2:4 decoder.

5. SIMULATION RESULTS

The implementation and simulation of the circuit were performed using the QCA Designer 2.0.3 software. Figure 9 shows the simulation results of a multilayer decoder. The simulation results are shown in table II.

TABLE II
DESIGN SPECIFICATION AND SIMULATION SETTING OF 2:4 DECODER

Cell Size	Cell Separation	Dot Diameter	Convergence Tolerance	Radius of Effect	Relative Permittivity	Clock High	Clock Low	Clock Amplitude Factor	Layer Separation
18nm × 18nm	2 nm	5 nm	0.001	65nm	12.50	9.8 e ⁻²² J	3.8 e ⁻²³ J	2.00	11.50 nm

Each majority voter gate needs one clock phase to function correctly. The buffer cell between the device cell and the output cell has allocated one clock with the output cell for reliability and creation of a correct output which is not affected by external factors, so the circuit needs three clocks. The proposed circuit consists of 100 cells, which shows a significant reduction relative to the previous designs. Reducing cell numbers will reduce the circuit occupied surface, reduce power consumption and increase the output signal level. According to the simulation results, only one of the outputs is 1 for each input pair, and the remaining outputs are in logic 0, indicating the correct operation of the circuit.

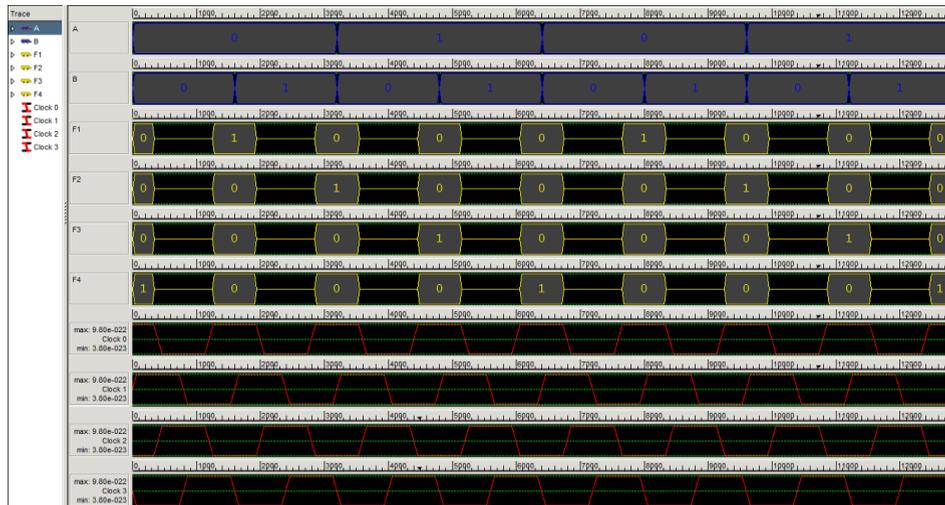


Fig. 9. Simulation results of the proposed 2:4 decoder.

In table III, a comparison has been made between the proposed design and the reference plan [21]. The comparison has been carried out based on the number of cells, the occupied surface, the number of gates, and the number of clock phases to produce the output, reflecting the improvement of the proposed plan compared to the previous designs.

TABLE III
COMPARISON BETWEEN THE PROPOSED CIRCUIT AND REF [22]

	Proposed Circuit	First Proposed in [25]	Second Proposed in [25]
Implantation Type	Multilayer	Coplanar	Coplanar
Cell Count	100	110	159
Area Covered (nm ²)	84824	129624	176872
Number of Gate	4	4	4
Clock Phases	3	3	3

6. CONCLUSION

QCA is a new computing technology and a possible replacement for CMOS technology. This technology has advantages such as lower power consumption, higher speed, and wiring-induced parasitic capacitors. QCA technology allows the implementation of all combinational logic circuits such as the full adder, subtractor, multiplexer, multiplier, and so on. In addition, sequential logic circuits such as the flip-flops, counters and memory cells can be implemented.

In this paper, the multi-layer architecture was provided for a 2:4 decoder using QCA technology. The use of multi-layer technique in QCA technology not only reduces the delay and the number of cells but also allows changing the design according to needs. This design operates in three clock phases and consists of 100 cells which cover a surface area of 0.88 μm^2 , which is significantly lower than the previous designs, leading to a decrease in the chip surface (despite the volume increase). Locating and evaluating circuit operation have been performed using QCA Designer software. Future research can be conducted on the advancement of better circuit design.

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