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A Novel Design of Penternary Inverter Gate Based on Carbon Nano Tube

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Abstract: This paper investigates a novel design of penternary logic gates using carbon nanotube field effect transistors (CNTFETs). CNTFET is a suitable candidate for replacing MOSFET with some useful properties, such as the capability of having the desired threshold voltage by regulating the diameter of the nanotubes. Multiple-valued logic (MVL) such as ternary, quaternary, and penternary is a promising alternative to the binary logic design, because of less complexity, less computational step and reduced chip area. We propose two penternary inverters which are designed in the multiple-valued voltage mode based on CNTFET. In the first proposed design, the resistors are used to implement penternary logic whereas, in the second proposed design, they are replaced with the transistors. Extensive simulation results using HSPICE represent that the two proposed designs reduce significantly the power consumption and delay and sensitivity to process variations as compared to the state-of-the-art penternary logic circuit in the literature.

Key words: CNTFET, Delay, Multiple-Valued Logic, Inverter, Penternary, Power Consumption.

1. INTRODUCTION

According to Moore's law, the number of transistors on a chip doubles approximately every 18 months. However, scaling down of the metal oxide semiconductor field effect transistor (MOSFET) leads to some problems and critical challenges such as short channel effect, increasing the gate leakage current, high power density [1-2]. To overcome these limitations, carbon nanotube field effect transistor has introduced a promising device due to the unique structure and excellent electrical properties [3]. The band gap of carbon nanotubes is an important parameter for the measurement of the threshold voltage (V_{th}) which is dependent on the nanotube diameter. Therefore, a multi-

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threshold circuit design can be done by using different diameters in the CNTFETs. The merits of CNTFETs enable to make low-power and high-performance logic gate.

The multiple-valued logic has interested among circuit and system designers. MVL circuits support more than two levels of logic. Using MVL circuits decreases power consumption, chip area, computation steps, and interconnection. Furthermore, MVL logic increases the bandwidth data transfer. Several studies have been accomplished in MVL logic gate and arithmetic circuits based on CNTFET. For instant, Raychowdhury *et al*. [4] designed the first ternary circuit based on CNTFET. They found that the ternary circuit requires $\log_2^3$ times less computation compared to the binary circuit. Lin *et al*. [5] proposed the modified ternary logic gate. They reported significant improvement in terms of power-delay product (PDP). Moaiyeri *et al*. [6] proposed new high-speed quaternary logic gates. In this paper, the novel design of ultra-low power penternary inverter gate based on CNTFET is proposed.

The rest of the paper is organized as follows: A brief review of CNTFET and multiple-valued logic for penternary logic are discussed in section 2. Two proposed of the penternary inverters are scrutinized in section 3. After that, the performance of the circuit through process variation is discussed in section4. Finally, in Section 5 conclusions are given.

2. REVIEW

A. *Brief Review of CNTFET*

Carbon nanotubes are formed by rolling the graphene sheets. They are classified into two groups which are called single-wall CNT (SWCNT) and multi-wall CNT (MWCNT).

The chiral-dependent properties of SWCNTs cause which behave metal or semiconductor. The chirality vector is represented by the integer pair (n, m). The nanotube is metallic if n=m or n-m=3i, where i is an integer. Otherwise, the nanotube is semiconductor. The semiconducting SWCNTs are employed as a channel of CNTFETs. The diameter of a CNT (D_{cnt}) in terms of (n, m) can be calculated as follows [11]:

$$D_{cnt}= 0.0783\sqrt{n^2 + nm + m^2} \quad (1)$$

Figure1 shows the structure of CNTFET. The CNTFET has four terminals. Doped CNT segments are placed between the gate and the source/drain, whereas undoped semiconducting nanotubes are placed under the gate as a channel region.

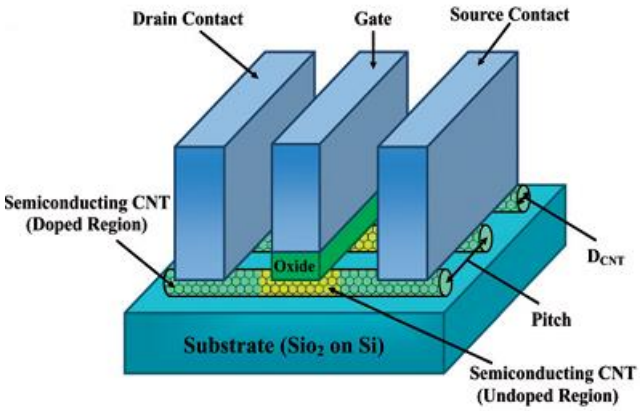

Fig.1. The structure of CNTFET.

The threshold voltage of CNTFET (V_{th}) is the required parameter to turn on the transistor [12-13]. V_{th} is defined as follows:

$$V_{th}=\frac{0.43}{D_{cnt}} \quad (2)$$

Where, D_{cnt} is the diameter of the CNT. CNTFETs provide a unique opportunity to control threshold voltage by changing the chirality vector, or the diameter of the CNT. In this paper, we use a multi-diameter CNTFET-based design for penternary logic implementation.

B. Review of MVL Design

If we consider f(X) as an m-valued n-variable function, where X={x_1, x_2, x_3, .., x_n} and each xi can get values from M={0,1,2,…, m-1}. Thus, f(X) is a mapping f: $M^n \rightarrow M$ and hence there are m^{m^n} different functions possible in the set f. Most common MVL is a ternary logic, which contains three significant logic levels. These logic levels include 0, $\frac{1}{2}Vdd$, and *Vdd* voltage levels. Similarity, the quaternary and penternary (five-valued) systems can be defined [14-18]. The quaternary logic includes 0, $\frac{1}{3}Vdd$, $\frac{2}{3}Vdd$, and *Vdd* voltage levels. Furthermore, the penternary logic includes $0, \frac{1}{4}Vdd$, $\frac{1}{2}Vdd$, $\frac{3}{4}Vdd$ and *Vdd* voltage levels. In order to reduce complexity in interconnection, power consumption, and fabrication cost [19-23], we propose a penternary inverter gate with only one power supply.

3. PROPOSED DESIGN

A. The First Design

The penternary logic includes five significant logic levels. These logic levels can be considered as 0, 1, 2, 3, and 4 symbols which are counterpart to 0, 1/4 *Vdd*, 1/2 *Vdd*, 3/4 *Vdd*, *Vdd* voltage levels. Table1 demonstrates the truth table of the penternary inverter.

TABLE I
Truth Table Of Penternary Inverter

Input	*Symbol*	*Out put*
0	0	*Vdd*
1/4 *Vdd*	1	3/4 *Vdd*
1/2 *Vdd*	2	1/2 *Vdd*
3/4 *Vdd*	3	1/4 *Vdd*
Vdd	4	0

The parameters of the CNTFET model [24] and their values and brief descriptions are given in Table II.

TABLE II
Characteristics of The Used CNTFET Model

Parameter	Brief description	Value
Lch	Physical channel length	≥10nm
Lss	The length of doped CNT source-side extension region	≥10nm
Ldd	The length of doped CNT drain-side extension region	≥10nm
Lgeff	The scattering mean free path in the intrinsic CNT channel and S/D regions	100nm
Pitch	The distance between the centers of two neighboring CNTs within the same device	20nm
Leff	The mean free path in p+/n+ doped CNT	≥15nm
Sub-pitch	Sub-lithographic pitch	≥4nm
Kox	The dielectric constant of high-k top gate dielectric material (HfO_2)	16
T_ox	The thickness of high-k top gate dielectric material	4
K sub	The dielectric constant of substrate (SiO_2)	4
C sub	The coupling capacitance between the channel region and substrate (SiO_2)	40 aF/μm
E_{fi}	The Fermi level of the doped S/D tube	6eV
Phi-M	The work function of source/drain metal contact	4.6eV
Phi-S	CNT work function	4.5 eV

The first proposed penternary inverter gate is designed based on CNTFET, which is shown in figure 2(a). This design consists of five CNTFETs with resistive pull-up. The resistors are used for making of accurate voltage levels.

The threshold voltages of CNTFETs are determined by Eq (2). The power supply voltage is 0.9V. The threshold voltage of an n-type CNTFET is 0.8, 0.56, 0.3, 0.12V respectively. For p-type CNTFET, the threshold voltage is 0.12V.

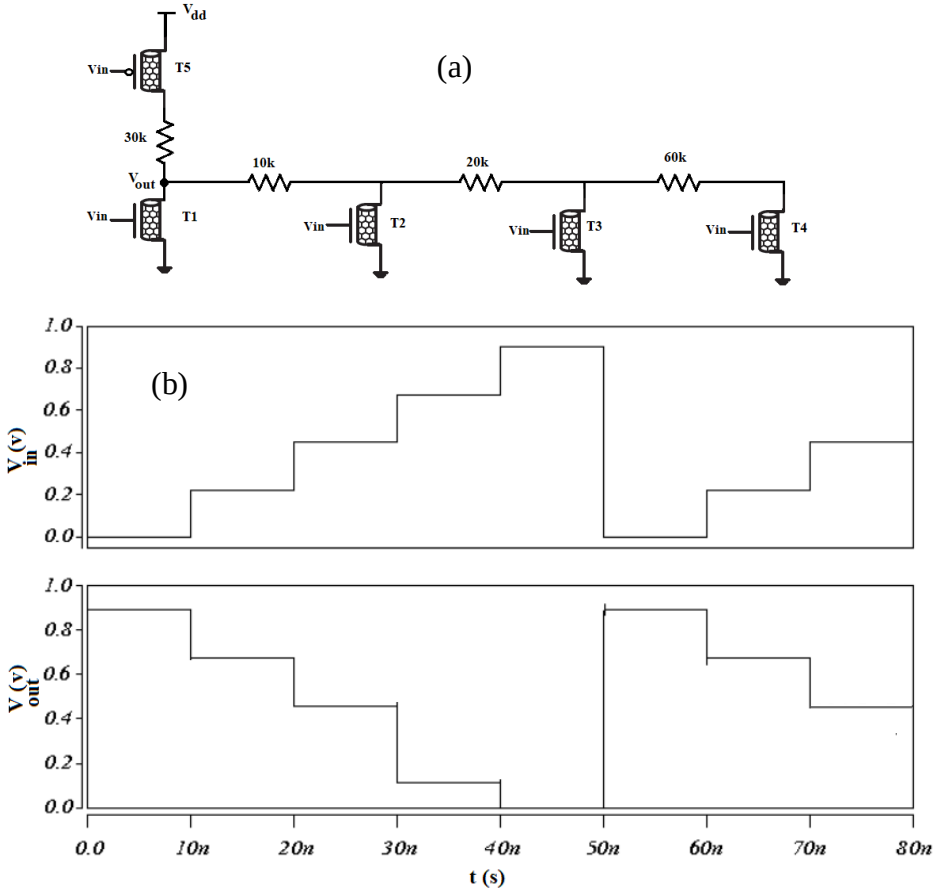

Fig. 2 a) The first proposed design. b) The transient response.

As seen in figure 2(a), when the input value is 0V, all n-type CNTFETs are off and only p-type CNTFET is on. Therefore, the output is *Vdd*. When the input value reaches around 1/4 *Vdd*, only T4 and T5 are on and the output is 3/4 *Vdd*. By increasing the input value to 1/2 *Vdd*, T4, T3, and T5 are turned on and the output becomes 1/2 *Vdd*. If the input value is around 3/4 *Vdd*, T4, T3, T2, and T5 are on and the output is 1/4 *Vdd*. Finally, if the input value is *Vdd*, all of CNTFETs are on and the output is 0V. The transient responses of the proposed design are demonstrated in figure 2(b).

B. The Second Proposed Design

In this design, the resistors are replaced with the proper transistor. The reason is that the resistor occupies the large area of the chip and causes difficulty for fabrication. Using the transistor reduces delay significantly. The second proposed design has the least PDP. Figure 3 shows the schematic of circuit design. T6, T7, T8, and T9 are the transistors that are replaced with the resistors. The chirality of these transistors is (19, 0).

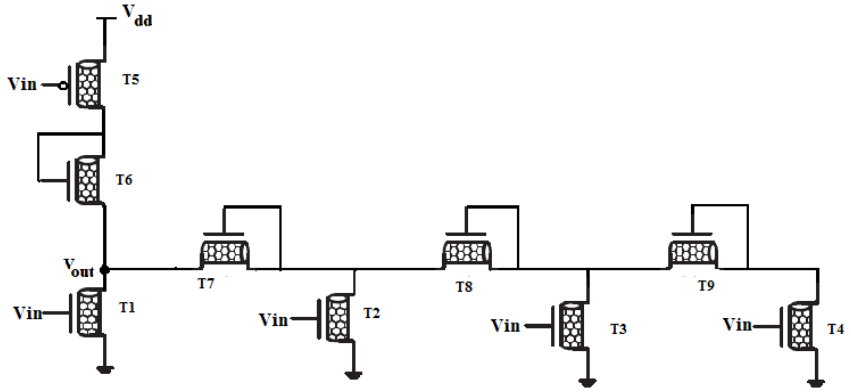

Fig. 3 The second proposed design.

In similar HSPICE parameter with the first design, results show that PDP of the second proposed design is 21.90×10^{-18} and the PDP of the first one is 88.9936×10^{-18}. The second design achieves more than 300% improvement over in terms of PDP. Furthermore, this design significantly improves than [18], [1]. The results are listed in Table III.

TABLE III
Simulation Results of The Penternary Inverter

Design	Power (e-6w)	Delay (e-12s)	PDP (e-18J)	Number of transistors
First proposed design	3.9225	22.688	88.9936	5
Second proposed design	3.7264	5.877	21.90	9
Ref [14]	3.41	7.85	267.685	14
Ref [1]	1.9560	65.126	127.3864	12

4. SIMULATION RESULTS AND DISCUSSION

The sensitivity to process variations and fabrication inaccuracies are the most important challenges in designing of nanoscale circuits. Therefore, variations of

oxide thickness, delay, and power consumption are examined.

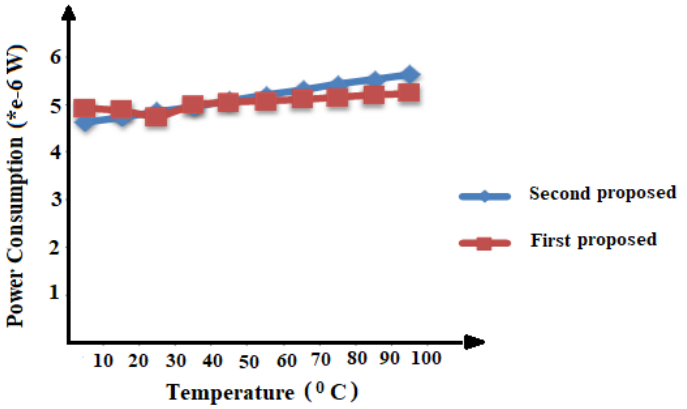

Fig. 4 Power consumption as a function of temperature.

As shown in figure 4, by increasing the temperature, power consumption remains unchanged.

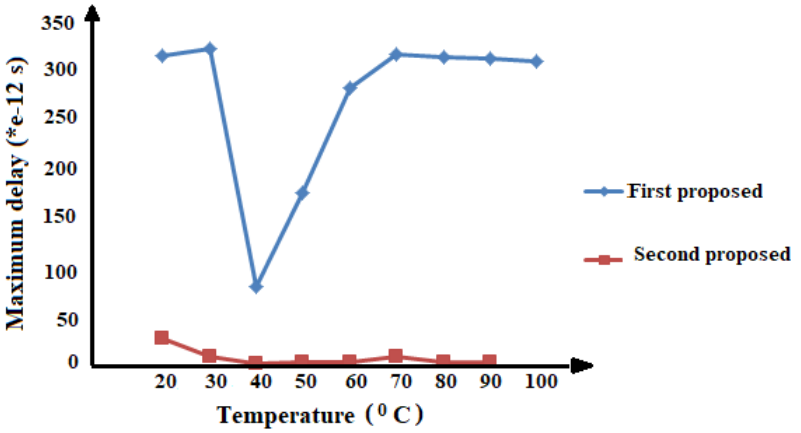

Fig. 5 Maximum delay variation as a function of temperature.

Figure 5 illustrates that the maximum delay as the function of temperature. The temperature changes range from 20 °c to 100 °c. For first design, the delay reduces in 40°c. In the second design, which has a lower delay, the variation is insensible.

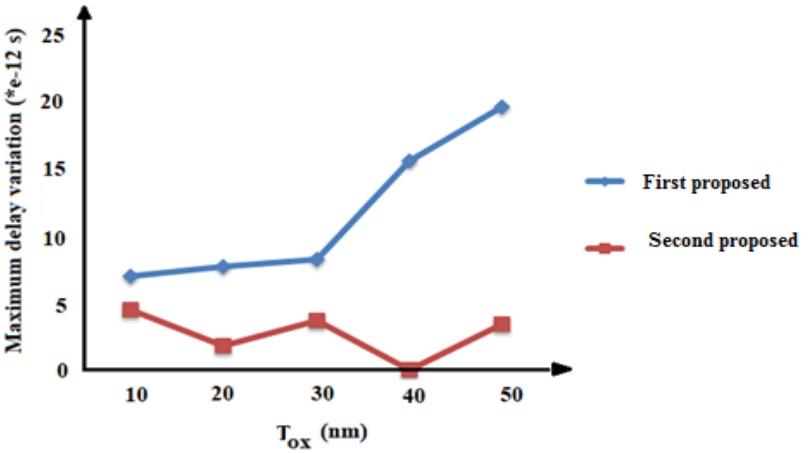

Fig. 6 Maximum delay as a function of Tox.

Figure 6 indicates the maximum delay versus Tox. As found in figure 6, by increasing the Tox, the maximum delay is increased in the first design. In the second design, the minimum delay is for Tox=40nm.

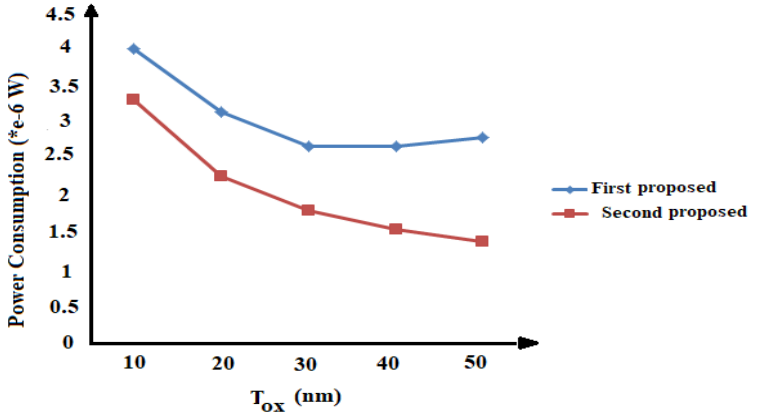

Fig. 7 Power consumption as a function of Tox.

The figure 7 exhibits that increasing Tox reduces the power consumption in both first and second designs.

5. CONCLUSION

We have proposed a new design for MVL design based on CNTFETs. The novelty of this paper lies in the fact that a new voltage-mode penternary inverter has been developed. In the first proposed design has been used the resistors by employing accurate voltage divider and the second proposed design contains the transistors which have been replaced the resistors. The Synopsys HSPICE

simulator has been used for examining the circuits. Simulation results show that the power consumption and PDP and sensitivity to process variations are reduced significantly as compared to existing penternary design. Both proposed designs have worked properly at different temperature and Tox. Increasing the temperature doesn't effect on the power consumption whereas, by increasing the Tox, the power and delay are reduced.

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